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## Transmission Line Matrix Modelling of Self Heating in Multi-finger 4H-SiC MESFETs

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**Abstract:** This study, presents a physical model with numerical simulations of self-heating in multi-finger 4H-SiC MESFETs. The model is based upon the parabolic heat diffusion equation. The governing equations and the associated boundary conditions are discretized and solved using the TLM method. Numerical simulations are presented for the case of six finger gate 4H-SiC MESFETs. Results show the effect of gate pitch and substrate thickness on temperature spreading and hot spot formation in the active area of the device. The transient by which steady state hotspot temperatures are reached is also considered.

**Key words:** SiC, MESFET, self heating, temperature, TLM

### INTRODUCTION

The microwave technology industry has used for many years the MESFET (Metal Semi Conductor Field Effect Transistor). This was mainly achieved in Silicon (Si) or Gallium Arsenide (GaAs). These two materials and other are used close to their physical limits, especially in terms of the power density. The wide band gap semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) attracted significant interest due to their physical and electrical properties (Quan-Jun *et al.*, 2008; Chattopadhyay *et al.*, 2008). Silicon Carbide (SiC) has been the object of a particular attention in last few years. The amelioration of the crystallographic quality of this material has allowed fabrication of high quality components. The first results gave hope for the fast advent of devices for applications in high power, high frequency and high temperature. SiC has the best physical and electrical properties for a semi-conductor in these domains such as high thermal conductivity ( $3\text{--}5 \text{ W cm}^{-1}\text{K}$ ), high electron saturation velocity ( $2.7 \times 10^7 \text{ cm sec}^{-1}$ ) and high breakdown electric field ( $2\text{--}4 \times 10^6 \text{ V cm}^{-1}$ ). Its wide band-gap makes it the perfect candidate to use for very high temperature operation, up to  $600^\circ\text{C}$  compared to Silicon ( $200^\circ\text{C}$ ) or Gallium Arsenic ( $300$  to  $400^\circ\text{C}$ ) (Hong-Liang *et al.*, 2008; Liu *et al.*, 2004; Dubuc, 2003). Recently Zhang *et al.* (2008) have demonstrated that the breakdown voltage can be improved up to 180% with inserting floating metal strips between gate and drain of a 4H-SiC Mesfet. This device is considered as one of the most important devices of the next generation for applications in high power, high frequency, high efficiency radio frequency and microwave electric circuits. For microwave circuit applications, high

voltage operation leads to ease of impedance matching in high power devices, thus allowing significant performance improvements and complexity reduction for high power devices and circuits (Song *et al.*, 2004). However, as any semiconductor component, the SiC MESFET is subject to problems of self-heating effects which increase the lattice temperature in the transistor channel and can significantly worsen the output characteristic of the transistor because of reduction in mobility and electron saturation velocity (Deng *et al.*, 2007). Knowledge of the temperature in the active area of 4H-SiC MESFETs is essential for optimizing device design, performance and reliability. Previous works on self-heating effect in 4H-SiC MESFETs has included Bertilsson *et al.* (2004) and Royet *et al.* (2000) who experimentally studied self heating and performed thermal simulations of SiC MESFETs in order to map the temperature distribution. In this work we develop a numerical model of self heating in multi-gate 4H-SiC MESFETs where we investigate the effect of gate pitch, substrate thickness and drain to source voltage on maximum temperature development. The model is based on the Transmission Line Matrix (TLM) method of Johns (1977) which has been successfully used for modelling diffusion phenomena (De Cogan and John, 1985; Smya *et al.*, 2001; De Cogan, 1998; De Cogan *et al.*, 2006). The TLM method is unconditionally stable, explicit and has considerable potential in the area of thermal simulation and design of semiconductor devices.

### STRUCTURE OF THE DEVICE

The device under consideration is shown in Fig. 1. The base material on which the transistor is fabricated is a thick 4H-SiC semi insulating substrate. A buffer layer is

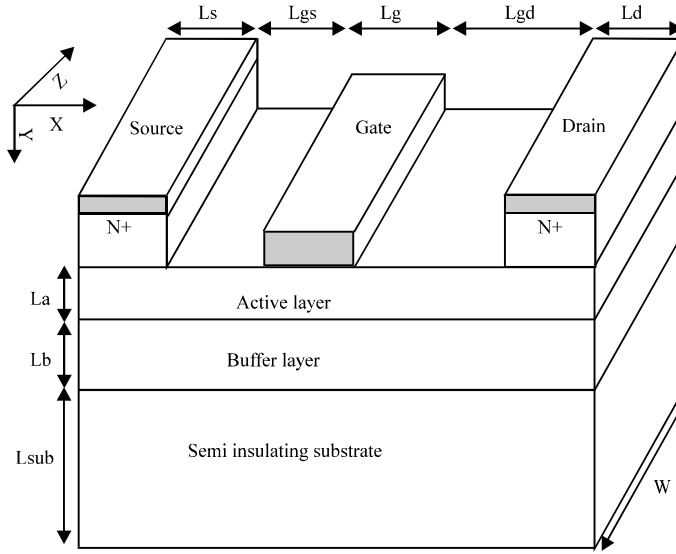


Fig. 1: A single gate 4H-SiC MESFET

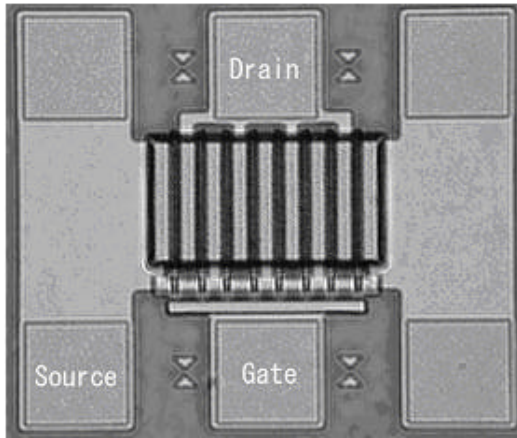


Fig. 2: Photograph of a multi-finger gate 4H-SiC MESFET

epitaxially grown over the semi-insulating substrate to isolate defects in the substrate from the transistor. The channel or the active layer is a thin, lightly doped (n) conducting layer of semi conducting material epitaxially grown over the buffer layer. Finally, a highly doped  $N^+$  contact layer is grown on the surface to aid in the fabrication of low-resistance ohmic contacts to the transistor. Two ohmic contacts, the source and drain, are fabricated on the highly doped layer to provide access to the external circuit. Between these two ohmic contacts, a Schottky contact, the gate, is fabricated. The source, drain and gate contacts are formed by metal. Although each of the source and drain contacts has negligible contact resistance, the gate contact makes an electrostatic

potential barrier (Schottky barrier) at the metal semiconductor contact without an external bias voltage (Royet *et al.*, 2000). The typical thickness and doping levels are:  $L_{sub} = 300 \mu m$  for the semi insulating substrate,  $L_b = 0.3 \mu m$  and  $N_a = 5.2 \times 10^{16} cm^{-3}$  for the p-type buffer layer,  $L_a = 1 \mu m$  and  $N_d = 1.6 \times 10^{17} cm^{-3}$  for the active layer,  $L_{N^+} = 0.2 \mu m$  and  $N_d = 1.1 \times 10^{19} cm^{-3}$  for the  $N^+$  contact layer. The gate length and width are, respectively  $L_g = 1.2 \mu m$  and  $W = 150 \mu m$ . The gate/source and gate/drain spacing are, respectively,  $L_{gs} = 0.5 \mu m$  and  $L_{gd} = 2.5 \mu m$ . Figure 2 shows Photograph of a multi-finger gate 4H-SiC MESFET.

#### HEAT GENERATION IN 4H-SiC MESFET

The physics of the schottky barrier is such that an effective negative potential is induced on the contact. This makes electrons move away from the region under the gate contact to the surroundings. Thus a depletion region, where the electron number density is much smaller than the rest of the active layer, is formed and the channel electrons can go through becomes narrow. When we apply a voltage between the drain and the source, most of the drain current flows in this narrow channel between the depletion region and the buffer layer. The thickness of the depletion region can be controlled by the gate-source voltage ( $V_{GS}$ ). If a negative  $V_{GS}$  is applied, the electrostatic potential barrier at the gate becomes higher and the thickness of the depletion region becomes bigger and the channel becomes very narrow resulting in a high electrical resistance between drain to source and in this manner the drain current is controlled. Figure 3 shows a schematic

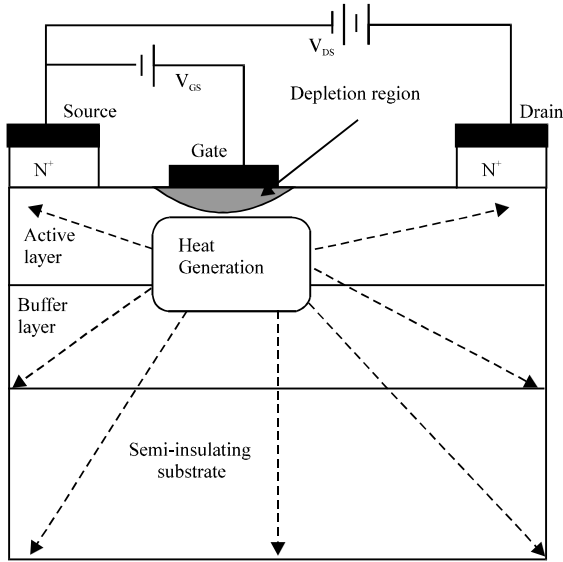


Fig. 3: Schematic diagram for heat generation in 4H-SiC MESFET

diagram of the heat generation mechanism in 4H-SiC MESFETs. When a voltage is applied between the drain and the source, electrons are accelerated from the source and flow within the channel to the drain. The electrons gain energy from the applied electric field and can become very energetic. Heat generation in semiconductor devices occurs due to the collisions between the electrons and the lattice within a restricted portion of the channel under the gate (Sze, 1981; Fushinobu *et al.*, 1995). Due to collisions, the lattice gains energy from the electrons that increases the lattice temperature in the transistor channel which can significantly worsen the current voltage characteristics because of the reduction in device parameters such as mobility and electron saturation velocity. Our objective, here, is to investigate aspects of the device's physical design that can influence the temperature spreading and the development of destructive hot spots.

### TLM MODEL

TLM method is an explicit and unconditionally stable technique which has a major benefit over other numerical techniques in that at all times during solution it retains a clear insight of the underlying physics of the phenomenon under investigation. It derives from the concept of using propagation delay in transmission lines as a time discretising element in a spatially discretised electrical network analogue of the physical problem. The telegrapher's equation for a three dimensional transmission line network is given by (Mimouni *et al.*, 2008):

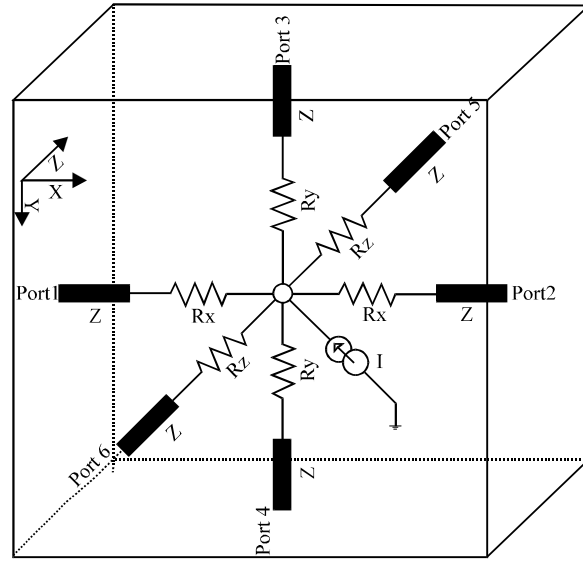


Fig. 4: A single 3D-TLM node with a current generator attached

$$\nabla^2 V = 6R_d C_d \frac{\partial V}{\partial t} + 3L_d C_d \frac{\partial^2 V}{\partial t^2} \quad (1)$$

where,  $V$  is the potential,  $t$  is the time,  $R_d$ ,  $C_d$ ,  $L_d$  are the distributed resistance, capacitance and inductance respectively. Conventional TLM models of heat diffusion consider the case where the time step is chosen to be sufficiently small for the second term on the right hand side of Eq. 1 to be negligible (Johns, 1977), so that Eq. 1 becomes analogous to the equation describing heat diffusion in a three dimensional homogeneous solid structure given by:

$$\nabla^2 T(x,y,z,t) = \frac{\rho C_p}{k_t} \frac{\partial T(x,y,z)}{\partial t} \quad (2)$$

where,  $k_t$  is the thermal conductivity,  $T(x, y, z)$  is the temperature at a point  $(x, y, z)$ ,  $\rho$  is the density of the material,  $C_p$  is the specific heat capacity and  $t$  is the time. Therefore, it is possible to model thermal diffusion processes in terms of a lumped RC network where temperature is represented by voltage and heat by current. In this technique the resistors remain clustered around the nodes, while the capacitance is modelled in terms of transmission lines that connect each node to its neighbours and carry pulses a finite distance  $\Delta x$ , in a finite time  $\Delta t$ . Figure 4 represents a single three dimensional TLM node including current generator to model the heat generation. These transmission lines have impedance:

$$Z = \frac{3 \Delta t}{C} \quad (3)$$

Using analogy between Eq.1 and 2, for each element of length  $\Delta x$ ,  $\Delta y$ ,  $\Delta z$ , the values of R and C are defined by:

$$\begin{aligned} R_x &= \frac{\Delta x}{2k_1 \Delta y \Delta z}; R_y = \frac{\Delta y}{2k_1 \Delta x \Delta z} \\ R_z &= \frac{\Delta z}{2k_1 \Delta x \Delta y}; C = \rho c_p \Delta x \Delta y \Delta z \end{aligned} \quad (4)$$

A TLM solution is obtained by considering voltage pulses,  ${}_k V_j^i(n)$  incident simultaneously on all parts of all nodes. These incident pulses are scattered instantaneously at nodes to become reflected pulses,  ${}_k V_j^r(n)$  which travel along link transmission line and arrive after a time  $\Delta t$  to neighbouring nodes. At each iteration and at each node, the nodal potential (Temperature),  ${}_k V(n)$  is calculated from the local sources and the incident pulses  ${}_k V_j^i(n)$  where  $k$  represent the  $k$ th iteration and  $j$  indicates the direction. For a three-dimensional node such as that illustrated in Fig. 4 when we apply the fundamental theorems of electricity, the nodal temperature at the  $k$ th iteration is given by Eq. 5:

$$\begin{aligned} {}_k V(n) &= \left[ \frac{2({}_k V_1^i(n) + {}_k V_2^i(n))}{R_x + Z} + \frac{2({}_k V_3^i(n) + {}_k V_4^i(n))}{R_y + Z} \right. \\ &\quad \left. + \frac{2({}_k V_5^i(n) + {}_k V_6^i(n))}{R_z + Z} + I(n) \right] \frac{1}{Y} \end{aligned} \quad (5)$$

where,  $I(n)$  represents the thermal current generator and  $Y$  represents the admittance which is given by:

$$Y = \frac{2}{R_x + Z} + \frac{2}{R_y + Z} + \frac{2}{R_z + Z} \quad (6)$$

The magnitudes of the scattered pulses are calculated from a circuit analysis of the nodes that gives:

$$\begin{aligned} {}_k V_{1,2}^r(x, y, z) &= \frac{1}{R_x + Z} [Z {}_k V(x, y, z) + (R_x - Z) {}_k V^i(x, y, z)] \\ {}_k V_{3,4}^r(x, y, z) &= \frac{1}{R_y + Z} [Z {}_k V(x, y, z) + (R_y - Z) {}_k V^i_{3,4}(x, y, z)] \quad (7) \\ {}_k V_{5,6}^r(x, y, z) &= \frac{1}{R_z + Z} [Z {}_k V(x, y, z) + (R_z - Z) {}_k V^i_{5,6}(x, y, z)] \end{aligned}$$

These reflected pulses travel to adjacent nodes along a transmission line and become incident pulses after a time  $\Delta t$ , so that:

$${}_{k+1} V_{jl}^i(x, y, z) = \rho_{jl} {}_k V_{jl}^i(x, y, z) + (1 - \rho_{jl}) {}_k V_{jl}^i(u, v, w) \quad (8)$$

Table 1: Values of  $j_1, j_2, u, v, w$  used for Eq. 8 and 9

$j_1$	$j_2$	$u$	$v$	$w$
1	2	$x-1$	$y$	$z$
2	1	$x$	$y$	$z$
3	4	$x$	$y-1$	$z$
4	3	$x$	$y-1$	$z$
5	6	$x$	$y$	$z-1$
6	5	$x$	$y$	$z+1$

where,  $\rho_{jl}(x, y, z)$  ( $j = 1, 2, \dots, 6$ ) represents the reflection coefficient in the direction  $j$  and is given by:

$$\rho_{jl}(x, y, z) = \frac{Z(u, v, w) - Z(x, y, z)}{Z(u, v, w) + Z(x, y, z)} \quad (9)$$

Values for  $j_1, j_2, u, v, w$  for Eq. 8 and 9 are listed in Table 1. For a continuous transmission line,  $p = 0$  but this will not be the case where adjacent elements have different associated capacitance and the pulse modification at the centre of each line takes account of this.

The TLM solution of the heat diffusion problem requires only the repeated solution of Eq. 5-9 with appropriate boundary conditions and appropriate time step:

- The boundary conditions express the interaction of the system at hand with its surroundings. Boundaries are part of the transport model and thus should be consistent with the description of the heat transport inside the medium. For an insulating boundary, any incident pulse will be returned equal in magnitude and in phase; this case correspond to an electrical open-circuit where  $Z(n+1)$  or  $Z(n-1)$  will be infinite and  $\rho_j = 1$ . For a heat sinking boundary, any incident pulse will be returned equal in magnitude but reversed phase, this case correspond to an electrical short-circuit where  $Z(n+1)$  or  $Z(n-1)$  will be zero and  $\rho_j = -1$ . (Kronberg *et al.*, 1998)
- The diffusion equation is really modelled by a transmission line only if the second term in the right hand side of Eq. 1 is negligible; this condition is generally satisfied by taking the time step  $\Delta t$  less than 10% of the value of the thermal time constant of the material. If the chosen value of  $\Delta t$  is too large, then there will be significant errors, some of them related to the increasing size of the double time derivative in Eq. 1, although the routine will remain numerically stable. (Johns and Butler, 1983; De Cogan and Shah, 1986)

In the current MESFET model, the drain current  $I_d = 190 \text{ mA}^{-1} \text{ mm}$  and drain voltage  $V_{ds} = 20 \text{ V}$  correspond to a power density  $P = 3.8 \text{ W mm}^{-1}$  (Zhang *et al.*, 2008). Heat generation which was represented by the current generator  $I$  in the TLM model, was defined for the fixed power density  $P$  in a small region under the gate on the

drain side. In this area, P is assumed to be dissipated uniformly and no heat generation is assumed elsewhere. Thermal boundary conditions were chosen such that all sides are adiabatic except the bottom of the device which was fixed to a heat sink at 300 K. For all simulations, a program was written in Matlab in order to evaluate the temperature within the device.

## RESULTS AND DISCUSSION

Figure 5a shows in xy plane the simulation results of the temperature distribution of a six finger-gate device with a uniform spacing of 50  $\mu\text{m}$  between fingers and

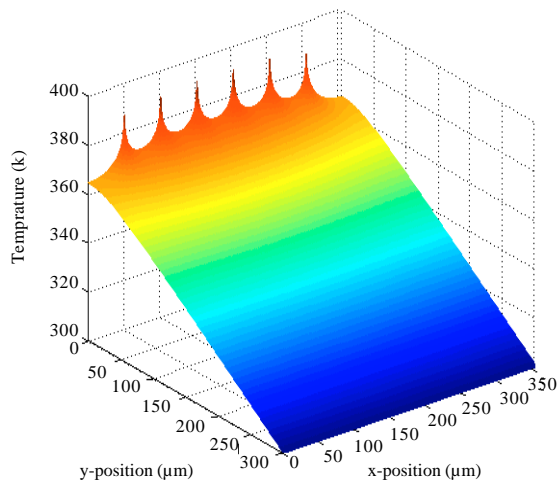


Fig. 5a: Temperature distribution on the xy plane of six finger-gate 4H-SiC MESFET

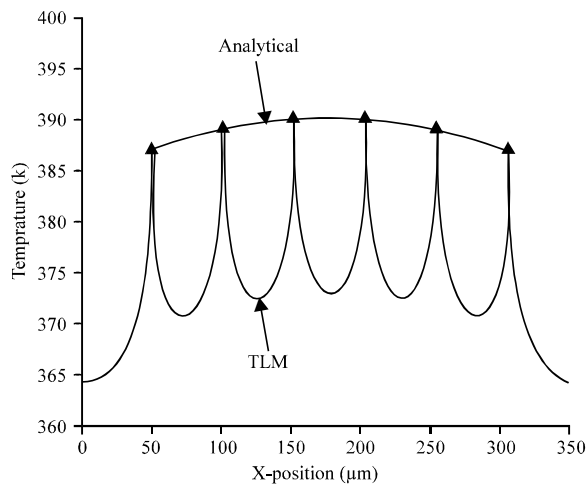


Fig. 5b: Temperature distribution along the top surface of six finger-gate 4H-SiC MESFET. Maximum values are compared with analytical predictions: -----Analytic, ----- TLM

300  $\mu\text{m}$  semi insulating substrate thickness. Each finger has a length of 1.2 and 150  $\mu\text{m}$  width. Maximum temperatures occur under each gate finger slightly off-centre and shifted towards the drain. Temperatures then fall towards the rear heat sink. Figure 5b plots steady the fingers is approximately 15 K. The maximum state temperatures in the upmost row of nodes, just under the gates. The temperature difference between each maximum and the neighbouring local minimum between temperatures are compared with those predicted analytically by Dubuc (2003) and they show good agreement.

Figure 6 illustrates how the maximum temperature in the channel varies with finger pitch. For a six finger device with  $V_{gs} = 0\text{ V}$  and  $V_{ds} = 20\text{ V}$  and substrate thickness of 300  $\mu\text{m}$ , hot-spot temperatures under gates 1, 2 and 3 (counting from outermost finger) are plotted against temperature for gate spacing varying from 10 to 60  $\mu\text{m}$ . The temperatures fall by nearly 260 K as the spacing increases, however, the temperature graph is clearly reaching a plateau by around 60  $\mu\text{m}$  spacing, suggesting that there would be little thermal benefit in increasing the finger pitch (and hence the device size) beyond this. The three graph lines corresponding to fingers 1, 2 and 3 lie very close together, with slightly more temperature difference as gate spacing increases. The inset shows that the difference in hot spot temperatures between fingers is approximately 3-4 K between fingers 1 and 2 and 1-2 K between fingers 2 and 3, for gate spacings of 35-50  $\mu\text{m}$ . Results for fingers 4, 5 and 6 are almost identical.

Figure 7 shows hot spot temperatures for finger 3 of the same device for substrate thickness 300, 200 and 100  $\mu\text{m}$ . The same conditions as before are considered: zero gate bias and 20V source-drain bias. Simulation results show clearly that decreasing the substrate thickness induces a decrease of temperature within the

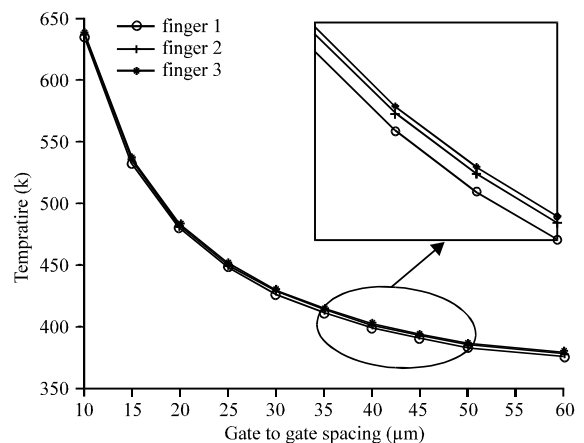


Fig. 6: Steady state temperatures of the hot-spots for a six finger-gate device

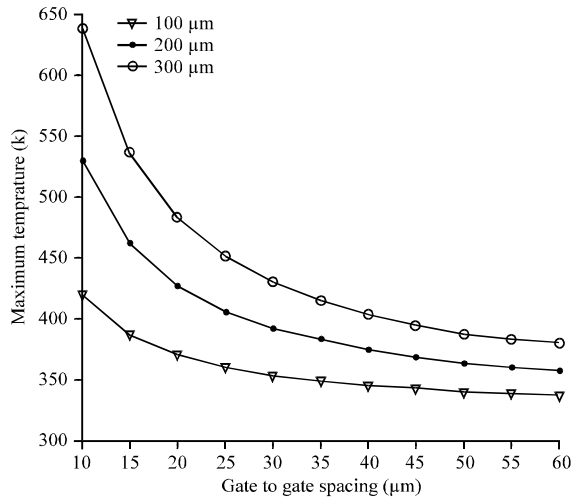


Fig. 7: Temperature distribution along the channel for three values of the substrate thickness

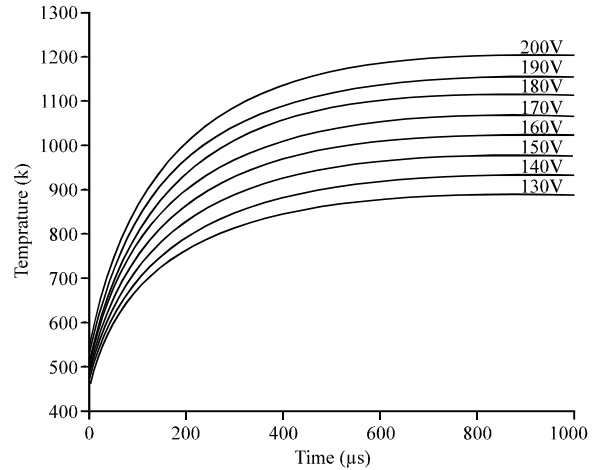


Fig. 9: Thermal transient of the hot spot beneath finger 3 for different values of Vds

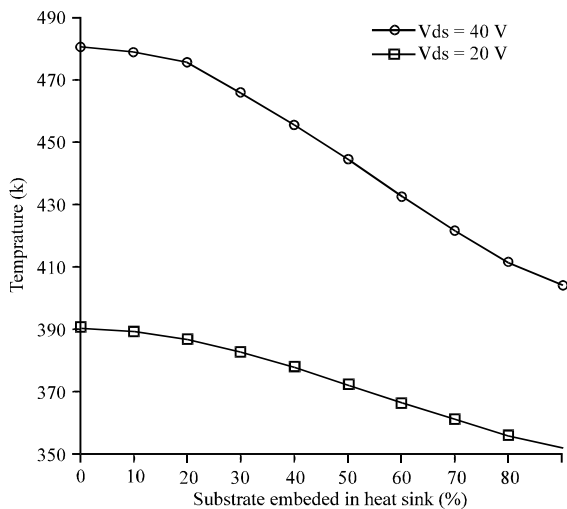


Fig. 8: Maximum steady state temperature in the channel of a six finger-gate 4H-SiC MESFET as function of percentage of substrate thickness in contact with the heat sink

channel of the device. From the Fig. 7, it can be seen that for 300  $\mu\text{m}$  substrate thickness, the hot spots temperature vary between 637.1 and 379.1 K when the finger pitch varies from 10 to 60  $\mu\text{m}$ , while for 100  $\mu\text{m}$  substrate thickness, the hot spots temperature vary just between 419.7 and 336.6 K. This is consistent with the fact that heat is generated closer to the heat sink as the substrate thickness decreases, so is more easily removed from the device.

Reducing substrate thickness increases the fragility of devices so, continuing the investigation of the effect of

the substrate on channel hot spots, we consider a six finger gate device with a uniform finger spacing of 50  $\mu\text{m}$  and a 300  $\mu\text{m}$  substrate, part of that substrate being allowed to protrude into the heatsink at 300 K. The simulation conditions are  $V_{gs} = 0$  but two values of  $V_{ds}$ , 20 and 40 V, are considered. Results are shown in Fig. 8 which plots maximum steady-state temperature in the channel against percentage of the area of the sides of the device in contact with the heat sink. This partial embedding is clearly beneficial in reducing channel temperatures, greater benefit being associated with higher power dissipations. The temperature reduction is likely to be caused by a combination of two effects: increasing the surface area of substrate in contact with the heatsink and bringing a portion of that contact area closer to the region in which heat is generated.

Figure 9 shows the temperature rise with time for the hot spot associated with finger 3 for different values of  $V_{ds}$ , obtained using a well converged model. Steady state temperatures are higher for greater values of  $V_{ds}$  and the temperature rise is more rapid during the transient. Since the maximum allowable channel temperature is 600°C (873 K) Dubuc (2003), Fig. 10 plots the time taken for hot spot temperature to reach 600°C versus  $V_{ds}$ . It appears that for  $V_{ds} = 130$  V the threshold temperature is not reached until 600  $\mu\text{s}$  into the transient, but this is reduced to 100  $\mu\text{s}$  at  $V_{ds} = 200$  V. This suggests that in pulsed operation a pulse associated with higher than typical values of  $V_{ds}$  can be tolerated from the thermal point of view so long as the pulse duration is sufficiently short and so long as the pulse is not repeated until the device has been allowed to cool.

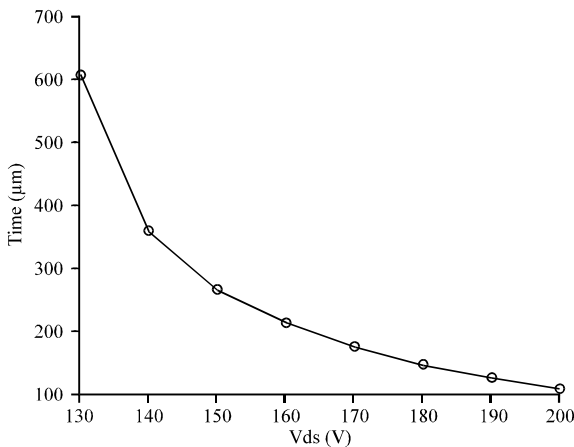


Fig. 10: Time taken for the hot spot associated with finger 3 to reach 600°C versus Vds

## CONCLUSION

Increased fingers spacing has been shown to bring about a dramatic reduction in steady state hot spot temperature, the effect starting to plateau at a spacing of 50-60  $\mu\text{m}$  for the geometry considered. Similarly, hot spot temperatures have been observed to fall when substrate thickness decreases and these falls are more dramatic when the fingers pitch is small. Since the issue of robustness limits how thin a substrate can be used, an alternative of placing the device in a shallow well in the heat sink so that portion of the device contacts the heat sink, has been investigated. This has also been shown to provide significant temperature reductions. Investigation of the transient by which hot spots reach their final temperature has shown that, for voltages which produce steady state hot spots above the threshold temperature of 600°C (873 K), it is still possible to operate at these voltages for realistic pulse durations so long as the pulses sufficiently spaced in time as to be independent from the thermal point of view. In this context, we comment on the fact that the same TLM model could be run with long time steps for the steady state simulation, without loss of stability, as well as with a short time step when high resolution and accuracy in the transient were needed.

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