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Reliability Improvement of the Analog Computer of a Naval Navigation System by Derating and Accelerated Life Testing

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Abstract: The reliability of the analog computer of the naval navigation system was improved by the application of derating and accelerated life testing. Spice circuit analysis and temperature profile analysis were performed based on which part derating scheme was developed. Afterwards a systematic approach for accelerated life testing was designed to discover the weaknesses of the system under test and the fixes to the system were performed to improve its reliability. Since many mechanisms of failure were present in the product being tested, the PMRL model was used for multiple failure modes in modeling the failure times obtained from accelerated life tests. A significant reduction in mean time to failure and improvement in reliability was achieved. The predictive calculations for the mean time to failures were carried out using MIL-HDBK-217F for the Naval Sheltered and the Naval Unsheltered working conditions per the real operating conditions of the system and were compared with the results obtained from our experimental and modeling work.

Key words: Reliability growth, electronic systems, derating, accelerated life testing

INTRODUCTION

The reliability of a system is affected by the reliability of its components and the way they are interconnected to serve its intended mission under certain operating conditions. The reliability of discrete components, analog circuits and their associated interconnects is very low. One may improve system reliability by using more reliable components, or system redesign using high reliability parts from newer technologies. Peiravi (2008) has shown that this can be realized by using filed programmable analog arrays. Another approach to increase the reliability of any electronic system is to use derating and accelerated life testing. In this study, the results of applying the latter approach to improve the reliability of the system under study are presented and it is shown how this can help to increase its mean time to failure and improve its reliability. Manufacturers of microelectronic devices often specify supply voltage limits and threshold values for power dissipation, output current, junction temperature and frequency. With these rated values known, a designer of electronic circuits who wishes to get a more reliable product may choose to lower these specifications. This practice of derating can provide an increased level of reliability since either stresses acting on a part are reduced or the strength of that part is increased by replacing it with a component with higher rated values. The history of this dates back to Arellano (1992) who presented an automated method of evaluating electronic equipment for overstress effects and derating implemented at Hughes Aircraft Company Many efforts were published later. Radu (2003) presented an example of stress derating and thermal analysis for a temperature controller as an example of an electronic system. He showed that performing derating before the components' placement and manufacture of PCBs assures proper component selection, saves redesign time and helps maximize circuit performance and reliability. Once derating is implemented, there is no way to prevent human errors, weaknesses in manufacturing and the possibility of using somewhat weaker components in the manufactured circuits. This would lead to a decrease in reliability and can only be dealt with through accelerated life testing. The main idea behind accelerated life testing is to expose the system under study to more severe stresses than their expected operating conditions. The system is going to wear out faster than usual and its weaknesses and lifetime can be determined in the laboratory. There are various ways to implement accelerated life testing which deal with how the increased stresses are applied. Van Dorp *et al.* (1996) developed a Bayes model for step-stress accelerated life testing using exponentially distributed failure times at each stress level. However, instead of using a strict time-transformation function, they used prior information to define a multivariate prior distribution for the failure rates at the various stress levels which helped preserve the natural ordering of the failure rates in both the prior and posterior estimates. Van Dorp and

Mazzuchi (2004) used their general Bayes inference model for accelerated life testing and inferred Bayes point estimates as well as probability statements for use-stress life parameters. The other problem with accelerated life testing is how to project the lifetimes obtained under accelerated test conditions to predict the real life of the device or system under test. The usual practice is reliance on the Arrhenius theory using activation energies. Hellstrom (2003) used these activation energies extensively in his thesis on accelerated life testing to study the effect of moisture on electrostatic discharge in electronic parts. He studied plastic encapsulated and open test circuits at different humidity and temperature conditions and derived an acceleration factor using the Arrhenius relation with which he determined failure rates at different conditions. This is somewhat questionable since there are various mechanisms of failure each of which may lead to a failure. Each failure mechanism has a different activation energy which makes it difficult to estimate the real lifetime. Thus it is difficult to decide which activation energy to use. When one tries to design accelerated life testing procedures for more and more reliable devices or systems which are supposed to operate at more extreme conditions, then the use of activation energies is somewhat questionable as presented in Petersen *et al*. (2002) where life tests were performed on indium gallium phosphide hetero-junction bipolar transistors (InGaP HBTs) with their junctions at 225°C for more than 1000 h and the devices showed no failure of significant degradation. The other problem is the modeling and qualification for failure when designing an accelerated life test for a certain product. Xijin (2006) presented modeling and qualification criteria for failure and accelerated life testing of cooling fans. Acevedo *et al*. (2006) reported that they performed accelerated life testing for critical hardware sub-assemblies used in telecommunication systems including power amplifiers, radio units and other sub-assemblies that have a strong impact on system reliability. They used accelerated life testing to evaluate potential product weaknesses and performance degradation over a simulated operational lifetime. Design changes were suggested to remedy these weaknesses prior to volume manufacturing and field deployment. They also used accelerated life testing to obtain statistical information to forecast the steady-state product reliability under the expected field conditions.

The system under test in this study was the analog computer of the gyrocompass in the navigational system of a naval vessel as reported by Peiravi (2008). It was shown that by integration of the analog computer using FPAAs system reliability improvement is achieved. This research done on the improvement of its reliability using derating and accelerated life testing is reported and it is shown that a major improvement in its reliability is achieved.

DERATING

The operating conditions of each part can seriously affect its reliability and life. Other factors including the production maturity and quality are also important in determining the failure rate of electronic components. These factors which are reported in the literature are shown in Table 1.

Using Table 1 one can easily see that derating could be used to reduce the failure rate. If in a given circuit, electronic parts of a higher rating than required in their operating conditions are used, then they have indeed been derated. This would reduce their failure rate drastically and lead to a decreased failure rate and an improved reliability. For example, the derating for a bipolar transistor is shown in Fig. 1.

In Fig. 1, the vertical axis shows the ratio of applied load to rated load at 40°C. The derating is determined from Eq. 1 where, S is the ratio of applied load to rated load at 40°C.

Table 1: The factors which affect the failure rate of electronic parts as reported in the literature

Components	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Digital and linear ICS		D			x		x	x	x				x	x	x
Hybrid circuits	D	D	D	D	D	x	x	x	x	x	x	x	x	x	x
Bipolar transistors		D	D			x	x	x	x	x	x	x	x	x	x
FETs		D	D			x	x	x	x	x	x		x	x	x
Diodes		D				x	x		x	x	x	x	x	x	x
Thyristors		D				x	x		x		x	x	x	x	x
Optoelectronic components		D		x	x		x	x	x				x	x	x
Resistors	D		D				x					x	x	x	x
Capacitors	D			D			x					x	x	x	x
Coils transformers	D		x	x			x						x	x	x
Relays switches	D			x	x		x	x		x	x		x	x	x
Connectors	D				x		x		x	x	x	x	x	x	x

1: Ambient temperature (θ_A), 2: Junction temperature (θ_J), 3: Power stress (S), 4: Voltage stress (S), 5: Current stress (S), 6: Breakdown voltage, 7: Technology, 8: Complexity, 9: Package, 10: Application, 11: Contact construction, 12: Range, 13: Production maturity, 14: Environment (π_E) and 15: Quality (π_Q), D: Denotes dominant, x: Denotes important

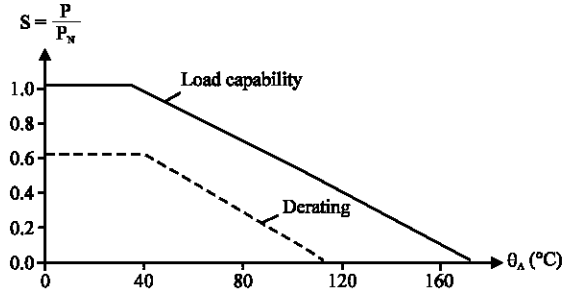

Fig. 1: Load capability and recommended derating of a bipolar transistor

$$S = \frac{\text{Applied load}}{\text{Rated load at } 40^{\circ}C} \quad (1)$$

In Fig. 1 the level of derating suggested is 40%. This varies from part to part and from application to application. There are some derating procedures suggested by various industries to fit their own needs. Although many recommendations have been reported for derating, our own derating procedure was adopted based on present application and design limitations.

ACCELERATED LIFE TESTING

There are various ways to apply stress in accelerated life testing. One may use constant stress models, step-stress or ramp-stress models. Chung *et al.* (2006) presented acceptance sampling plans based on failure-censored step-stress accelerated life tests for parts with Weibul life distributions. Bai and Chun (1991) presented optimum simple step-stress accelerated life tests (ALTs) for products with competing causes of failure. They assume that the life distribution of each failure cause is independent of the others and is assumed to be exponential with a mean that is a log-linear function of the stress and a cumulative exposure model is assumed. A progressive step-stress plan was applied in this research as shown in Fig. 2 with both positive and negative temperature cycles. The system was started out in the chamber at 25°C and its temperature was raised to 85°C in a ramp and then down to -25°C in order to cover the commercial electronics part temperature cycle. The system was held at each temperature level for nearly 5 min to allow it to stabilize and tested. Then it was cooled down for 5°C to let any solder joint failure mechanisms to show up. It was reheated again to its previous level and retested. Five degree step changes were used on both sides in order to overstress out parts. The cycles were repeatedly applied until a failure was observed. The system under test was electrically active during the whole test time and any failure was immediately recorded.

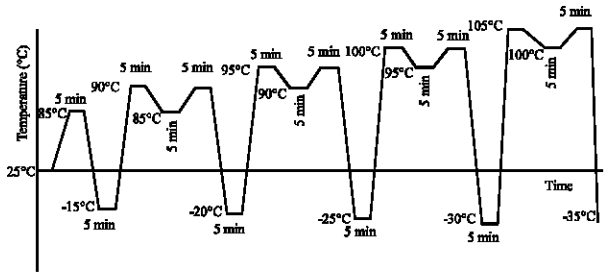

Fig. 2: Progressive step-stress plan applied for present accelerated life test

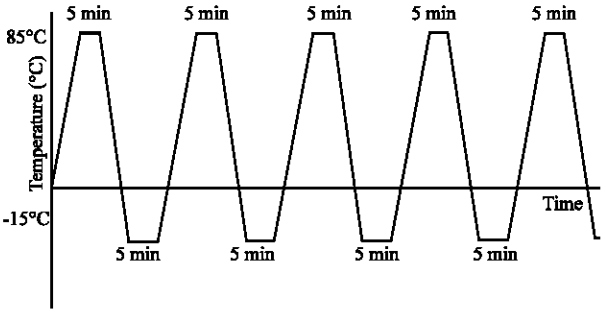

Fig. 3: Application of temperature stress through several cycles

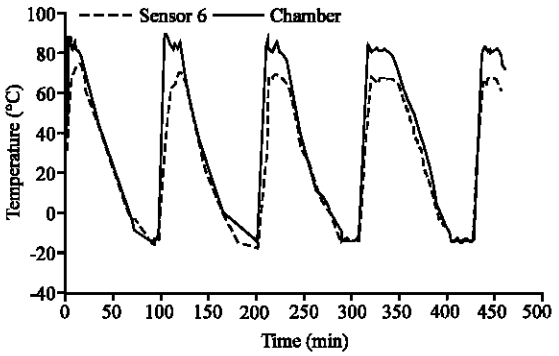

Fig. 4: The temperature of sensor 6 compared with that of the chamber in an accelerated life testing experiment

Once we ran the above tests, we found our design weaknesses and fixed them. In the next step we started out with present system at room temperature and then applied ramp stress cycles which took present system up to +85°C and held it there for at least 5 min and then brought it back down to -15°C and held it there for at least 5 min (Fig. 3). We repeated this cycle until failure was observed.

The temperature in the chamber were the accelerated life testing is carried out is not exactly the same as we desire since many factors such as the geometry of the chamber, the size and physical characteristics of the circuit being tested and the thermal characteristics of the heating and cooling system all affect the temperature profile. Of course not all the parts in the chamber follow the applied temperature profile exactly as we wish. For example, we show a sample of the measurements of temperature of one of the sensors in present experiments in comparison with the chamber temperature in Fig. 4.

RELIABILITY OF THE SYSTEM UNDER TEST

Reliability of electronic circuits has been a major concern especially in important subsystems of naval vessels and military apparatus. The reliability is the probability of successful operation during the mission and under pre-specified conditions. Since naval vessels must operate at sea, the general conditions for which electronic subsystems of naval vessels are evaluated are the Naval Sheltered and the Naval Unsheltered as per MIL-HDBK-217F (1995). The failure rates for the parts which make up the electronic circuits can also be either estimated based on the generic rates of MIL-HDBK-217F or other data sources. The reliability can be calculated using various techniques including RBD, Markov state space, analytical, or Monte Carlo Simulations. We used the RBD technique along with failure rate data from MIL-HDBK-217F. For example, the general failure rate for a resistor is:

$$\lambda_p = \lambda_b \, \pi_T \, \pi_p \, \pi_S \, \pi_Q \, \pi_E$$

where, λ_b is the base failure rate, π_T is the temperature factor, π_p is the power factor, π_S is the power stress factor, π_T is the quality factor and π_E is the environment factor. There is a similar relationship for other devices with appropriate factors to include stresses and operating environment.

EXPERIMENTAL RESULTS

The circuits in the analog computer mostly consisted of metal film resistors, cermet trimmer potentiometers, polyester capacitors, glass diodes, transistors, op-amps, regulators plus the printed circuit and interconnections. The data from MIL-HDBk-217F (1995) was used for the failure rates of the electronic parts of the system under study. We obtained the following results:

λ_{NU} = 180.203242FPMH
λ_{NNS} = 54.04694FPMH

The circuits were integrated into a new one using several discrete components and TRAC020 FPAA. The system was first integrated using software to redesign the I/O interface. Then it was implemented and tested. The new system was much smaller in volume and weight and much more reliable than the original system. This study was reported by Peiravi (2008). The data from MIL-HDBK-217F was used for the failure rates of the electronic parts of the system under study before derating or accelerated life testing. We obtained the following results:

λ_{NU} = 150.168176FPMH
λ_{NNS} = 44.253FPMH

Then, we applied derating to the parts by performing an exact spice circuit analysis and temperature profiling analysis and used our own derating policy. Once derating was applied to the parts the failure rate was considerably reduced and we were able to obtain a considerable reduction in the failure rate. We obtained the following results:

$\lambda_{NU\text{-derating}}$ = 116.545521FPMH
$\lambda_{NNS\text{-derating}}$ = 33.344635FPMH

Further improvements in the reliability were achieved once accelerated life testing was performed. By the application of the temperature stress cycling tests presented above, we found weaknesses in assembly plus the weak components. We proposed changes in assembly procedures and changed the weak components with more reliable ones. We ran the accelerated life tests again on the modified versions and obtained the average lifetime by repeated experiments. The expected lifetime under stressful conditions was experimentally determined and then the average failure rate prediction for the normal operating conditions was computed using present PMRL model and the following results were obtained:

$\lambda_{NU\text{-accel-life-test}}$ = 94.666018FPMH
$\lambda_{NNS\text{-accel-life-test}}$ = 26.808467FPMH

DISCUSSION

In this study, the results of derating of the various electronic components of the analog computer of the gyrocompass of a naval vessel and accelerated life testing have been presented and the improvement in reliability is demonstrated. The comparison of the failure rate from Table 2 shows an improvement in reliability after both derating and accelerated life testing. A 35.32% improvement was achieved in the Naval Unsheltered case

Table 2: The percent reduction of the failure rate of the analog computer before and after integration by FPAA, derating and accelerated life test (in failures per million hours)

Case	Failure rate in the naval sheltered case (FPMH)	Percent improvement in reliability measure	Failure rate in the naval unsheltered case (FPMH)	Percent improvement in reliability measure
Analog computer before integration by using FPAA	54.046940		180.203242	
Analog computer before derating	44.253000	18.12	150.168176	16.67
Analog computer after derating	33.344635	38.30	116.545521	35.32
Analog computer after accelerated life testing	26.808467	50.39	94.666018	47.46

and a 38.30% improvement in the Naval Sheltered case for derating. A 47.46% improvement was achieved in the Naval Unsheltered case and a 50.39% improvement in the Naval Sheltered case after accelerated life testing. This show the additional benefits of derating and accelerated life testing over integration of the parts with which we had already reported an achievement of 16.67% improvement in the Naval Unsheltered case and an 18.12% improvement in the Naval Sheltered case.

CONCLUSIONS

In this study, we have presented the results of derating and accelerated life testing of the various circuits of the analog computer of the gyrocompass of a naval vessel and showed the improvement in reliability. We showed a 35.32% improvement in mean time to failure for the Naval Unsheltered case and a 38.30% improvement in the mean time to failure of the Naval Sheltered case after derating. We also showed a 47.46% improvement in the mean time to failure of the Naval Unsheltered case and a 50.39% improvement in the mean time to failure of the Naval Sheltered case as a result of changes done after accelerated life testing. We encountered several problems in the design of the laboratory setup for our accelerated life tests for which we proposed long term solutions pending proper funding. We also proposed a future study to consider the effect of multiple failures on the test results which requires new methodology as well as changes in our experimental setup. This has been proposed as the next step in present research.

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