Journal of Applied Sciences

ISSN 1812-5654

science alert

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Journal of Applied Sciences 7 (18): 2568-2575, 2007
ISSN 1812-5654

Automatic Design of Micropower CMOS Voltage Controlled Oscillator (433 MHz) for PLL Application

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Abstract: This study deals with the design of a voltage controlled oscillator designed to be part of a Phase Locked-Loop (PLL), which implements the frequency synthesizer of a Low-IF transceiver. The transceiver operates in the European 433-MHz ISM band. We focus on low-cost, low-voltage (1... 1.5V) battery operated systems to be used in portable applications (medical care, surveillance systems...). Therefore we want the analog cells to be fully integrated in a single chip solution. In the design of the VCO we developed a Top-Down strategy, starting from high-level specifications such as consumption, operating frequency and phase noise and subsequently deriving transistor sizes and bias. This present study will begin with a look at the basic delay cell operation, including the replica bias circuit used to establish the output swing. Performance as a function of process technology will be considered. The conclusions from this Top-Down methodology will be applied to the design of ring-oscillator inverter delay cells in a 0.35 μm CMOS process. The complete design sequence for the delay cells will be described and transistor sizes determined.

Key words: Ring VCO, PLL, power consumption, top-down methodology

INTRODUCTION

The most important parameters of an implanted biotelemetry system are size and power dissipation. A significant portion of the power budget for any implantable telemetry system is allocated to the generation of the RF carrier. Given the need for small, low-power wireless devices for biotelemetry, a low-power, integrated frequency synthesizer is required.

The major sources of power dissipation in CMOS PLL synthesizer are the VCO (73%) and the frequency divider (22%). The VCO's power dissipation is determined by the frequency of operation and the phase noise performance required (Nathan *et al*., 2005).

Many novel delay cells of ring oscillator- based VCOs have been proposed recently to minimize the timing jitter, phase noise and power consumption (El-Hage and Yuan, 2004; Eken and Uyemura, 2004).

The realization of VCOs with good supply noise rejection, low power consumption and high frequency capability requires careful attention to circuit design issues.

This study presents a methodology to automatically evaluate the specifications of VCOs.

This review leads to an automatic synthesis algorithm developed in MATLAB which systematically transits from high level specifications to the VCO specifications and then to transistor sizing.

The method which we will choose to calculate optimal dimensions of transistors will be related to a high level specifications required by the final application and the system in which the circuit is integrated.

Let us recall that the VCO should be used in a transmitter with 433 MHz. The objects can be multiple for RF applications.

In our concerns, we particularly interest to minimize the consumption and our dimensioning method was developed accordingly.

The dimensioning strategy is based on gm/I_D methodology developed by D. Flandre for micropower OTA optimisation (Silveira *et al*., 1996).

The proposed methodology considers the relationship between the transconductance over drain current ratio (gm/I_D) and the normalized drain current ($I_D/(W/L)$) as a fundamental design tool.

This methodology has been widely used since its publication proving its advantages in analog circuits design particularly to obtain reasonable power-speed compromise.

In this study this methodology is extended to optimize ring VCO performances.

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TOPOLOGY OF THE RING VCO

We present here the general topology of the ring oscillator while taking into account the number and type of cells used.

The architecture selected for the VCO is consisted on setting in cascade four stages with an odd number of inversions (Fig. 1).

This differential delay cell used PMOS load transistors called loads of Maneatis (Kim *et al*., 1990) made up of 2 PMOS transistor in parallel: A PMOS in linear region and a PMOS of the same size connected in diode. This provides a more linear output resistance, over the entire range of the output voltage swing, than a simple PMOS in linear mode. It also guarantees good performance over process variation and improve the performances of the VCO in term of phase noise (Hajimiri *et al*., 1999).

Circuit of coarse tuning control: The basic differential delay cell is shown in Fig. 2. It features a source coupled differential pair with resistive loads which are implemented by PMOS transistors.

A replica biasing circuit is used to adjust the gate bias of the PMOS load devices for a fixed swing at the output. A simplified schematic of the replica biasing circuit is shown in Fig. 2.

In this circuit a current source with the same magnitude (or current density) used in the differential delay cell draws current from a replica of the PMOS load transistor. A feed back loop using a simple operational amplifier gain block sets the PMOS gate bias voltage so that with the full I_B flowing through the load device a drain-to-source voltage of V_{SW} is seen across it. This gate bias voltage is drives the loads in the differential delay cells, resulting in a DC swing of V_{SW} for each side (total differential output swing of $2V_{SW}$).

Since the VCO must be included in a PLL, the VCO gain must be low enough to ensure the stability of the PLL and to minimize the effects of noise. Two types of tuning range must then be foreseen: A coarse tuning range with low gain and a fine tuning with high gain.

Two circuits of adjustment were thus envisaged on the design of ring oscillator VCO: A circuit of strong adjustment and a circuit of precision adjustment.

This circuit can be used to set the swing at the appropriate level over a wide range of supply and biasing conditions. The nominal time delay per stage in a delay chain employing such elements is $t_d = Ct\ R_L$.

The load capacitance Ct seen at the output consists of the gate-to-source capacitance of the next stage, the

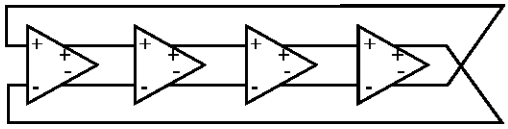

Fig. 1: Structure of ring VCO

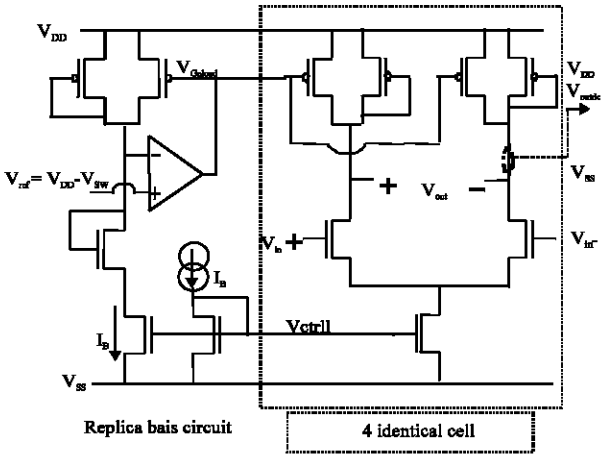

Fig. 2: A simplified schematic of coarse tuning control circuit

drain-to-gate capacitance of the triode load, as well as drain to bulk parasitic capacitances and wiring capacitances.

If the current source, I_B is swept over a range of values and the swing is held constant by the replica bias, then a wide range of frequencies can be attained. This gives the ring-oscillator a wide coarse tuning range. In effect, by changing the current and allowing the replica biasing circuit to adjust the gate bias for the triode load, we are tuning the resistance of the output load device.

The period of a ring oscillator with N delay stages is approximately 2N times the delay per stage. This translates to a centre frequency of

$$f = \frac{1}{2N \cdot t_d} = \frac{I_B}{2N \cdot Ct \cdot V_{SW}} \quad (1)$$

A useful substitution is made by noting that the term I_B/V_{SW} is actually the reciprocal of the effective resistance of PMOS load R_L called loads of Maneatis. R_L supposed sufficiently linear and is worth in this case:

$$R_L = \frac{V_{SW}}{I_B} = \frac{V_{DD} - V_{outdc}}{I_B/2} \quad (2)$$

Where, V_{DD} is the voltage supply and V_{outdc} is the DC component of voltage swing signal.

We see immediately how the frequency of oscillation can be controlled while acting on the value of bias current I_B and thus by tuning the resistance load R_L.

Fortunately, differential delay cells with a triode load (and replica biasing) are easily tunable over a wide range of frequencies. The current per stage can be tuned over a wide range while the replica bias adjusts the resistance of the load so that a fixed swing, V_{SW}, is maintained. The range over which this approach works depends primarily on the range of resistance values that can be achieved in the triode load by varying its (V_{GS}-V_T) bias point.

Considering that the resistance of a Maneatis load is roughly equal to pMOS resistance of the same size in linear region, the small signal resistance of the PMOS load as a function of V_{Gpload} is given by

$$R_L = \frac{1}{\mu_p C_{ox}\frac{W_p}{L_P}\left(nV_{outdc} - V_{Gpload} - \left|V_{T0pload}\right| + (1-n)V_{DD}\right)} \quad (3)$$

Therefore the range of output resistances that can be tuned is bounded by $V_{Gpload,max}$ et $V_{gpload,min}$.

A wide range of frequencies is attainted with V_{DD} = 1.5V and V_{TO} = 0.617V according to 0.35 um CMOS process.

A high VCO gain imposes constraints on the range of PLL design parameters such as the gain (or attenuation in the loop filter) and the gain of the phase detector. Therefore, it is desirable to use a combination of coarse and fine tuning.

Circuit of fine tuning control: The fine tuning technique is needed for the PLL voltage control path. This can be achieved by steering additional current I_{tune} into the delay cells which is not mirrored in the replica triode device, as illustrated in the simplified schematic in Fig. 3.

In this circuit the differential control voltage input V_{ctrl2} drives a differential pair and steers some portion of additional biasing current I_{ctrl} through a current mirror into the delay cell devices. The nominal total current of polarization of each cell is given by
$I_B = I_C + I_{tune}$, I_C being the current duplicated in the circuit of coarse tuning control.

Benefits of this approach include a differential control voltage input which is compatible with differential implementations of the loop filter and charge pump circuits preceding the VCO.

To first order, increasing the current in the delay cells would have no effect on the frequency of the output. This is because the time delay per stage t_d, depends on the ratio of V_{SW} to I_B. If the load where actually a linear resistor then increasing the current would increase the swing proportionally and the time delay per stage would remain

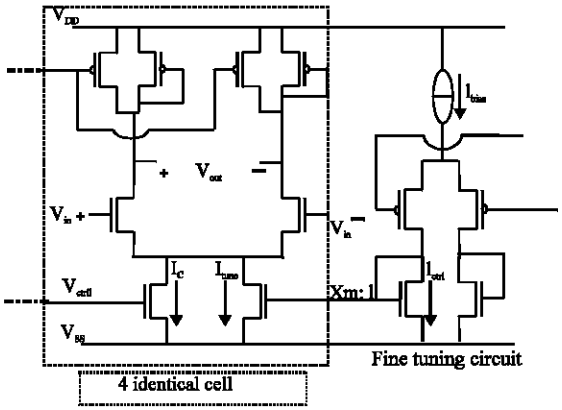

Fig. 3: A simplified schematic of fine tuning control circuit

constant. With the triode device, however, there is a second order variation, in the output swing with respect to changes in current.

This non-linearity allows the VCO to be tuned over a small range through variations in the supply current.
The VCO gain is given by

$$K_{VCO} = \frac{\partial f_0}{\partial V_{ctrl2}} \cong \frac{\partial f_0}{\partial I_{tune}}\frac{\partial I_{tune}}{\partial V_{ctrl2}} = \frac{\partial f_0}{\partial I_{tune}}\frac{\partial I_{ctrl}}{\partial V_{ctrl2}}Xm \quad (4)$$

where, I_{tune} is the amount of additional current being supplied to the delay cells (and not to the replica) and Xm is the ratio of device sizes in the current mirror in Fig. 3, which is also the ratio of I_{tune} to I_{ctrl}.

The total tuning range of the VCO accessible through the control voltage path is given by

$$\text{Tuning range} \approx \frac{\partial f_0}{\partial I_{tune}} I_{bias} \cdot Xm \quad (5)$$

METHODOLOGY OF VCO OPTIMIZATION

Once the architecture of VCO defined, we have developed a top-down methodology to define the sizes and bias of the different transistors constituting the VCO.

The method which we will choose to calculate optimal dimensions of transistors will be related to a high level specifications required by the final application and the system in which the circuit is integrated.

Let us recall that the VCO should be used in a transmitter with 433 MHz.

The objects can be multiple for RF applications. In our concerns, we particularly interest to minimize the consumption and our dimensioning method was developed accordingly.

Secondarily, we also took care to minimize total surface and phase noise.

Here, we describe the methodology of dimensioning which we developed. We treat in the order the differential cells, the circuit of coarse tuning control and the circuit of fine tuning control.

Optimisation of the differential cells: The dimensioning method of the differential pairs is illustrated on Fig. 4; it is based on gm/I_D methodology (Silveira *et al.*, 1996). W and L are the widths and lengths of transistors channel. Indices N and pload respectively refer to the transistors NMOS of differential cells and the PMOS of load. All parameters of the circuit (dimensions, polarizationY) are deduced in a univocal way from W_{pload}, L_{pload} and Ln. The initial choice of those is made so as to ensure a minimization of the consumption.

Calculation of DC component of voltage swing: The choice of output swing, V_{SW}, is influenced by several competing factors. At the top level there is the trade-off between speed, which favors low output swing and noise margins, which favor high.

There are also considerations related to regions of transistor operation which limit how large of an output swing is useful.

A first limit on the output swing comes from the differential pair transistor with a high input voltage requires a large enough V_{ds} to remain in saturation ($V_{Gn} \le V_{T0n} + nV_{Dn}$).

An excessive swing is also disruptive from the perspective of the other transistor in the differential pair. In fact, the NMOS drain of a cell is connected to the gate of one of both NMOS of the following cell. Let us consider the limiting values which the drain voltage can take. On the assumption that the differential pairs switch completely, those are equal:

$$V_{Dnmax} = V_{DD}$$
$$V_{Dmin} = V_{DD}\text{-}V_{sw} = V_{DD}\text{-}2(V_{DD}\text{-}V_{outdc}) = 2V_{outdc}\text{-}V_{DD}$$

If we consider the critical case $V_{Gn} = V_{dnmax}$ and $V_{Dn} = V_{Dmin}$, the transistors remain saturated if V_{outdc} being higher than minimal value:

$$V_{outdc} \ge \frac{V_{DD}(1+n) - V_{T0n}}{2n} \quad (6)$$

Second, it is desirable to keep one of the tow PMOS constituting Maneatis load transistors in the triode region of operation.

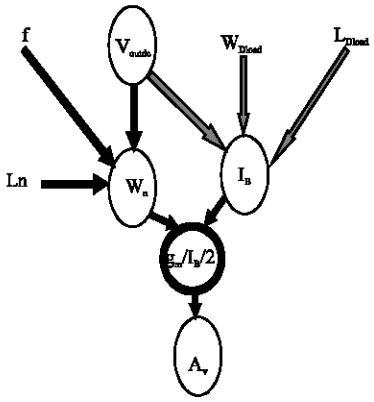

Fig. 4: A symbolic dimensioning algorithm of differential pairs

This requires a drain voltage that respects the following constraint:

$$V_{Dpload} = V_{Dn} \ge V_{Dsat} = \frac{V_{Gpload} + V_{T0p} + V_{DD}(n-1)}{n} \quad (7)$$

Or $V_{Dpload,min} = 2V_{outdc}\text{-}V_{DD}$

We thus find the second constraint imposed on the value of V_{outdc}:

$$V_{outdc} \ge \frac{V_{T0pload} + V_{DD}(2n-1)}{2n} \quad (8)$$

Regarding to these previous constraints we can define an interval of values allowed for V_{outdc}.

The V_{outdc} voltage was fixed in the middle of the interval of acceptable values. For example, V_{outdc} is fixed at 1.34 V for a supply voltage of 1.5 V.

Calculation of I_B: Once the value of V_{outdc} fixed, the following stage of our dimensioning consists in calculating the value of the bias current I_B of the cells according to the frequency of oscillation F, V_{outdc}, W_{pload} and L_{pload} (Fig. 4).

To calculate current I_B, we must initially determine the V_{Gpload} of the PMOS in linear region. This voltage must be lower than:

$$V_{Gpmax} = V_{DD} - |V_{T0pload}| - 2n(V_{DD} - V_{outdc}) \quad (9)$$

The minimum value of V_{Gpload} is $V_{Gpmin} = V_{SS}$.

Let us recall that the gate voltage of the PMOS is regulated by the replica bias circuit to ensure a constant amplitude oscillation whatever the frequency. Thus we took:

$$V_{Gpload} = \frac{V_{Gpmax} - V_{Gpmin}}{2} \quad (10)$$

Once the gate voltage of the PMOS is fixed, I_B can be calculated as being the sum of the currents of the PMOS in linear and the PMOS in diode of the Maneatis load.

The value of the drain current I_{D1} of the PMOS in linear can result directly from their dimensions W_{pload} and L_{pload}.

(11)

$$I_{D1} = \mu_p C_{ox} \frac{W_{pload}}{L_{pload}} (V_{DD} - V_{outdc}) \left[V_{DD}(1-n) - |V_{T0p}| V_{Gpload} + \frac{n}{2}(V_{outdc} + V_{DD}) \right] \quad (11)$$

The drain current of the transistor P assembled in diode in saturated mode is given by the following equation:

$$I_{D2} = \mu_p C_{ox} \frac{W_{pload}}{L_{pload}} \frac{1}{2n} (V_{DD} - V_{Gpload} - |V_{T0pload}|)^2 \quad (12)$$

The value of current I_B can be deduced from the Eq. (11) and (12) since $I_B/2=I_{D1}+I_{D2}$

Calculation of Wn: As indicated in Fig. 4, Wn can be deduced from the oscillation frequency f (Eq. 1), the bias current I_B, calculated in the preceding section and Ln, fixed a priori. From the choice of the dimensions of the Maneatis load PMOS transistors we can derive the value of R_L from (Eq. 3). We then calculate the dimensions of the NMOS transistors of the differential pairs such that the capacitance Ct at the output nodes allows us to achieve the desired oscillation frequency 433 MHz.

The load capacitance seen at the output consists of the gate-to-source capacitance of the next stage, the drain-to-gate capacitance of the triode load, as well as drain to bulk parasitic capacitances and wiring capacitances.

These capacitances are evaluated by using EKV model (Chan and Chen, 2003; Porret *et al.*, 2001) giving continuous expressions from weak to the strong inversion.

The EKV model proposes, for example, C_{gb} and C_{gs} empirical analytical expressions which are valid in and continuous between all regimes of operation. Figure 5 illustrates this modeling as a function of V_G as well as g_m/I_D.

Calculation of the voltage gain AV: The gain can be calculated starting from the parameters and sizes defined previously:

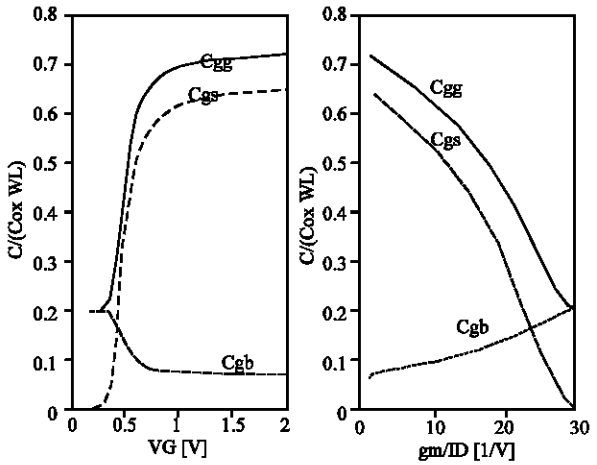

Fig. 5: EKV modeling of intrinsic gate capacitance as a function of gate voltage

$$Av = g_{m,n} R_L = g_{m,n} \frac{V_{DD} - V_{outdc}}{I_B/2} = \left(\frac{g_m}{I}\right)_n (V_{DD} - V_{outdc}) \quad (13)$$

Where, $g_{m,n}$ is the gate transconductance of the NMOS

It was suggested previously that the gain per stage needs to be sufficiently larger than one for the ring-oscillators to oscillate. The gain should be sufficiently high to insure oscillation over a range of different process and temperature conditions.

In the analysis of timing jitter (Hajimiri *et al.*, 1999), however, it was concluded that higher gains are not beneficial. Therefore the gain is kept as small as possible, while leaving a sufficient safety margin for process and temperature variations.

The choice of V_{outdc} was already discussed. In order to determine the transistors sizes of load W_{pload} and L_{pload} as well as the length Ln of the NMOS, We use MATLAB implementation of our dimensioning algorithm (Fig. 4) to choose the optimal values of those sizes. The adequacy and potential of VCO regarding our purpose will be discussed.

A numerical illustration (Fig. 6) of this design approach implemented on MATLAB by including the physical and technological parameters fixed by the 0.35 μm MOS fabrication process analyses the VCO performances.

An increase in W_{pload} has a harmful influence on the bias current I_{cell} and thus on the power consumption. On the other hand a reduction in W_{pload} reduces the voltage gain A_V. We will thus choose W_{pload} width as small as possible ensuring a sufficient gain.

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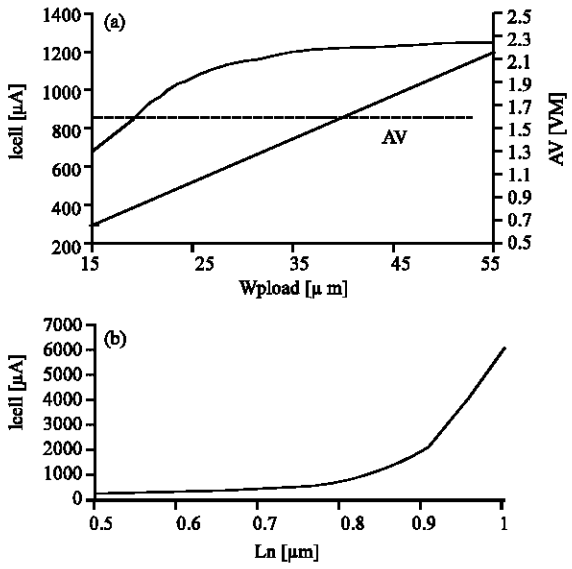

Fig. 6: Results of MATALB simulation, (a): The voltage gain and the bias current as a function of W_{pload} and (b): The bias current as a function of Ln

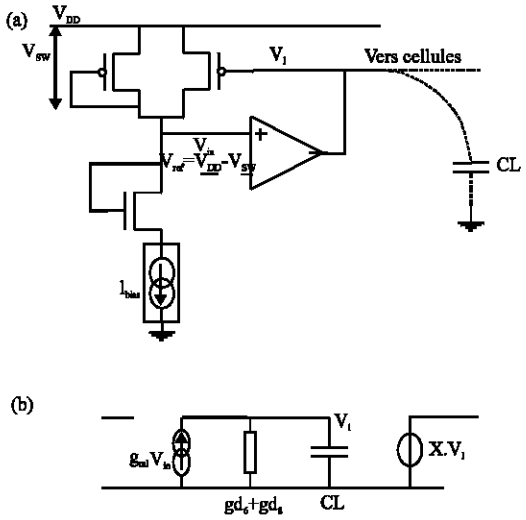

Fig. 7: (a) Coarse tuning circuit (b) Small signal schematic of the open loop with OTA

On the other hand a reduction in W_{pload} reduces the voltage gain A_V. We will thus choose W_{pload} width as small as possible ensuring a sufficient gain.

Simulations on MATLAB make it possible to show for a constant gain A_V, an increase on the L_{pload} length implies an increase in consumption. On the other hand, it is also favourable from the point of view of consumption to decrease Ln as much as possible, the minimal value being fixed by technology.

Optimisation of coarse tuning control circuit: The OTA constituting this circuit was dimensioned according to the method suggested in (Ayed *et al.*, 2005).

The OTA current mirrors were designed to repel the parasitic poles and zeros sufficiently beyond the transition frequency in order to ensure a margin of phase higher than 60° and thus to ensure the stability of the loop.

The loop of feedback in which is integrated it the OTA and the small signals schematic of the open loop are illustrated in Fig. 7.

The DC gain Av and the product gain bandwidth GBW in open loop are equal to those of OTA multiplied by a factor X:

$$\begin{aligned} A_{v0,BO} &= A_{v0,OTA}X \\ GBW_{BO} &= GBW_{OTA}X \end{aligned} \quad (14)$$

The factor X is given by:

$$X = \frac{\partial V_{Dpload}}{\partial V_{Gpload}} = -\frac{\partial V_{sw}}{\partial V_{Gpload}} \quad (15)$$

Optimisation of fine tuning control circuit: Figure 8 presents the method followed to dimension this circuit (Fig. 8).

The nominal total bais current of each cell is given by $I_B = I_C + I_{tune}$, I_C being the current controlled by the circuit of coarse tuning and I_{tune} controlled by the circuit of fine tuning,

The expression of the gain [Hz/V] is given by the Eq. (4).

The conductance value of the differential pair is deduced from the value of the gain:

$$g_m = \frac{2K_{VCO}}{\frac{\partial f_0}{\partial I_{tune}}Xm} \quad (16)$$

The drain current I_{ctrl} drain of the differential pair is known:

$$I_{ctrl} = \frac{I_{tune}}{Xm} = \frac{I_B/2}{Xm} \quad (17)$$

The value of the ratio gm to I_D is thus known and is worth:

$$\left(\frac{g_m}{I_D}\right)_{source} = \frac{4K_{VCO}}{\frac{\partial f_0}{\partial I_{tune}}I_B} \quad (18)$$

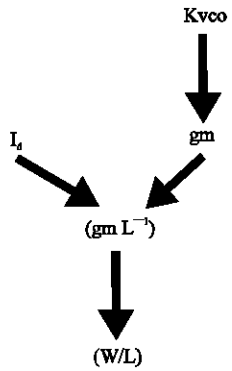

Fig. 8: A symbolic dimensioning algorithm of fine tuning circuit

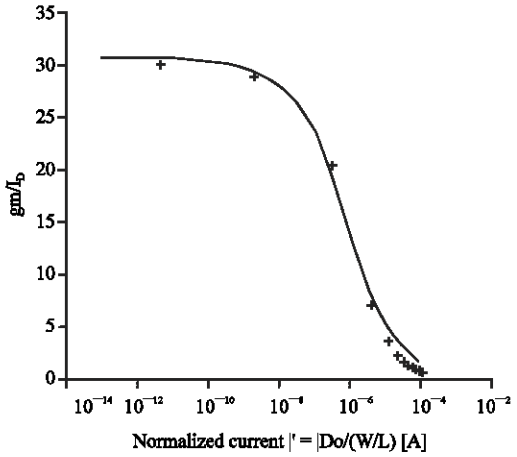

Fig. 9: Transconductance-over-drain current ratio vs normalized drain current

The EKV model provides a simple expression for the gm/I_D ratio as a function of the normalized current $I' = I_D/(W/L)$. The relation given by EKV model only depends on the technological parameters, not on the exact transistor dimensions. The quality of this empirical gm/I_D modeling is demonstrated on Fig. 9 by the excellent agreement with an experimental characteristic measured on a typical 0.35 μm MOS transistor.

From the gm/I_D value given by the previous equation the normalized drain current can be deduced using EKV model:

$$\frac{I_D}{W/L} = \frac{I_{ctrl}}{W/L} = I'_{ctrl} \quad (19)$$

The ratio W/L of the transistors constituting the differential pairs of the fine tuning circuit is calculated then in the following way:

Table 1: Simulated performances

Parameters	Values
Nominal frequency	433 MHz
Minimum transistor length	0.35 μm
Supply Voltage	1.5 V
Number of cells	4
Cell consumption	0.8 mW
Load capacitance	100 fF
Voltage swing	300 mv
Phase noise at 500 Khz Offset	100 dBc/Hz

$$\frac{Wfine}{Lfine} = \frac{Ictrl}{I'ctrl} \quad (20)$$

The value of the gain K_{VCO} is chosen in order to ensure the stability of PLL which the VCO is integrated in.

CONCLUSIONS

Simulations with a CMOS AMS 0.35 μm technology yield the results given in Table 1.

This methodology of dimensioning was implemented on MATLAB and applied to a CMOS AMS 0.35μm technology. We notice that our procedure of dimensioning is independent of technology and conduit to an optimal solution from the point of view of consumption.

The sizes of the transistors as their bias points are calculated starting from high level specifications such as consumption, the oscillation frequency and the phase noise.

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