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A Novel Low Power and High Performance 14 Transistor CMOS Full Adder Cell

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Abstract: Full adders are important components in applications such as Digital Signal Processors (DSP) architectures and microprocessors. Demands for the low power VLSI have been pushing the development of aggressive design methodologies to reduce the power consumption drastically. To meet the growing demand, The present study propose a new low power adder cell by sacrificing the MOS Transistor count that reduces the serious threshold loss problem, considerably increases the speed and decreases the power when compared to the Static Energy Recovery Full (SERF) adder. So a new improved 14T CMOS l-bit full adder cell is presented in the present study. Results show 50% improvement in threshold loss problem, 48% improvement in speed and considerable power consumption over the SERF adder and other different types of adders with comparable performance.

Key words: Arithmetic circuit, full adder, low power, very large-scale integration (VLSI)

INTRODUCTION

The adder is one of the most critical components of a processor, as it is used in the arithmetic logic unit (ALU), in the floating-point unit and for address generation in case of cache or memory access (Shalem *et al*., 1999). Increasing demand for mobile electronic devices such as cellular phones, PDA's and laptop computers requires the use of power efficient VLSI circuits. There are two basic approaches to reduce power consumption of circuits in scaled technologies: reducing the dynamic power consumption during the active mode operation of the device and the reduction of leakage current during the stand-by mode (Zimmermann and Fichtner, 1997). The power consumption of a CMOS digital circuit can be represented as

$$P = f C V_{dd}^2 + f Ishort V_{dd} + Ileak V_{dd} \quad \text{---------- (1)}$$

Where f is the clock frequency, C is the average switched Capacitance per clock cycle, V_{dd} is the supply voltage, Ishort is the short circuit current and Ileak is the off current (Zimmermann and Fichtner, 1997). In a well-optimized low power VLSI circuit, the 1st term of Eq. 1 is by far the dominant.

The stand-by power consumption is accounted for by the 3rd term. Using a lower V_{dd} is an effective way to reduce the dynamic power consumption since the 1st term is proportional to the square of V_{dd}. It should also be noted that the short circuit and leakage power dissipation are also strongly dependent on V_{dd}.

The lower the supply voltage is, the smaller the power consumption. However, using a lower V_{dd} degrades performance. The conventional adder uses 28 transistors implemented in CMOS technique shown in Fig. 1.

A new full adder called Static Energy-Recovery Full adder (SERF) uses only 10 transistors shown in Fig 2, which has the least number of transistors and is reported to be the best in power consumption, according to (Shalem *et al*., 1999).

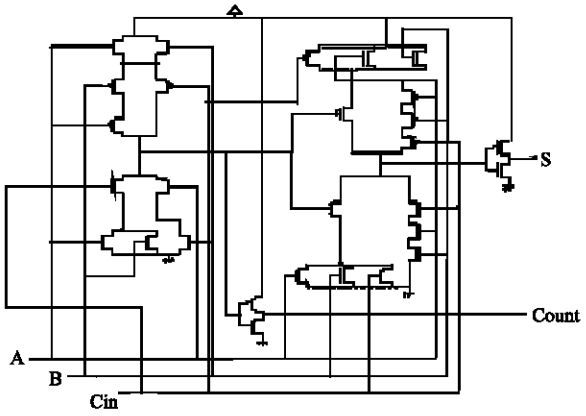

Fig. 1: 28-transistor CMOS adder schematic

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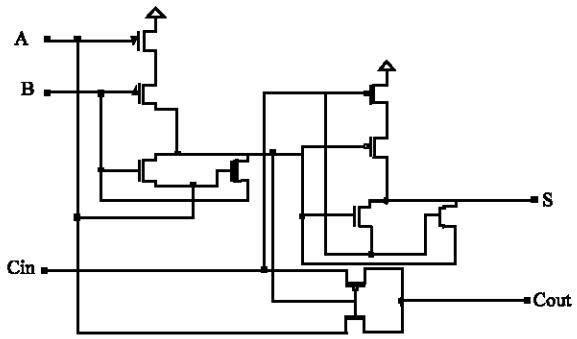

Fig. 2: Static Energy Recovery Full (SERF) adder

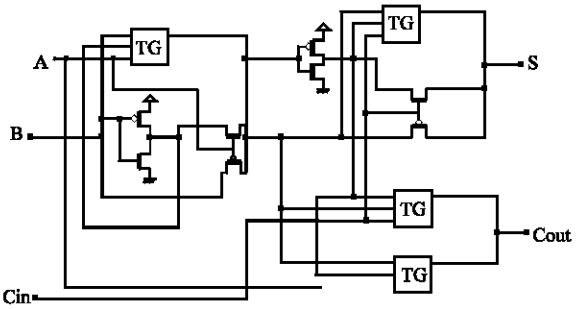

Fig. 3: The Transmission Function Adder (TFA)

Many low-power adders using various pass transistors, such as the SERF (Shalem *et al*., 1999) Compared to The complementary static CMOS adders, such low-power adders have the problem of threshold loss, i.e., the logic value 1 is not the value of V_{dd} and the logic value 0 may not be the value of 0. This kind of threshold-loss logic gates may not be used as widely as the complementary static CMOS gates. However, they are certainly useful in building up larger circuits such as multiple-bit input adders and multipliers. In this study we propose a new approach to designing many 14-transistor full adders. The aim of present study is to reduce the threshold-loss problem which exists in earlier designs (Shalem *et al*., 1999); however, our new adder cells are useful for designing larger circuits such as multipliers despite increase in transistor count by four per cell.

MATERIALS AND METHODS

Previous work: The full adder operation can be stated as follows: Given the three 1-bit inputs A, B and Cin, it is desired to calculate the two 1-bit outputs Sum and Cout, where

Sum = (A xor B) xor Cin
Cout = A and B + Cin . (A xor B)

Several designs of low power adder cells can be found in the literature (Shalem *et al*., 1999; Weste and Eshraghian, 1993; Zimmermann and Fichtner, 1997). The transmission function full adder (Zhuang and Wu, 1992), which uses 16 transistors, for the realization of the circuit, is shown in Fig. 3. For this circuit there are two possible short circuits paths to ground. This design uses pull-up and pull-down logic as well as complementary pass Logic to drive the

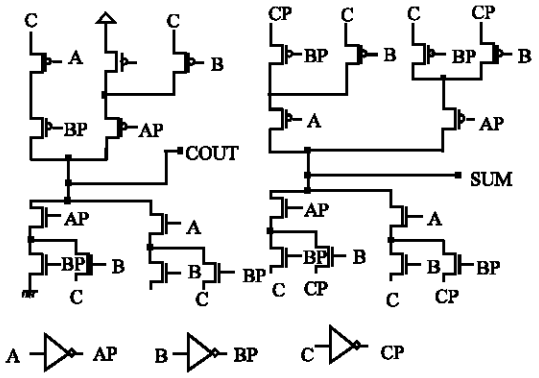

Fig. 4: The Dual Value Logic (DVL) adder

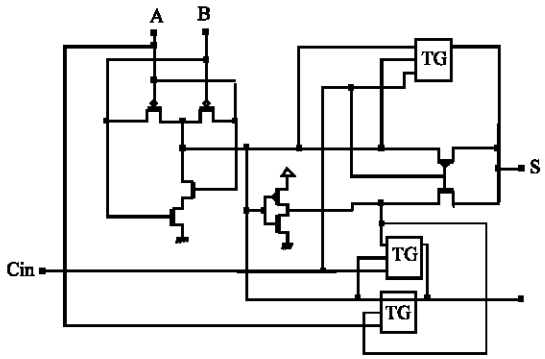

Fig. 5: The fourteen Transistor (14T) adder

load. The Dual Value Logic (DVL) full adder (Oklobdzija *et al*., 1995) shown in Fig. 4 uses 23 transistors for the realization of the adder function. The DVL was developed to improve the characteristics of double pass transistor logic, which was designed to have the logic level high signal passed to the load through a P-transistor and the logic level low Drained from the load through an N-transistor. The Fourteen transistors full-adder (Ahmed and Bayoumi, 1998), as the name implies, uses 14 Transistors to realize

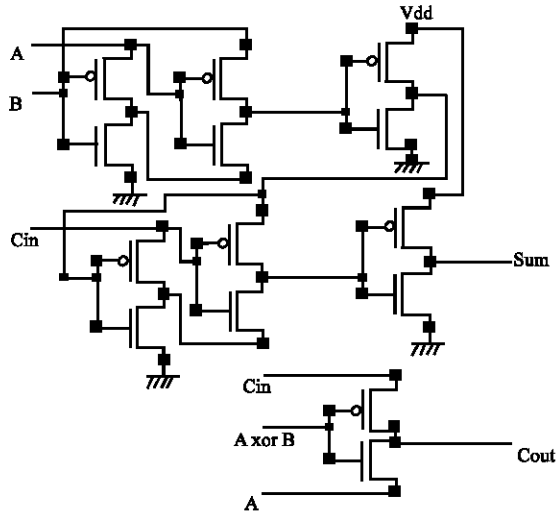

Fig. 6: New improved 14T Adder

the adder function (Fig. 5). The 14T full adder cell, like the transmission function full adder cell, implements the complementary pass logic to drive the load. The SERF design requires only 10 transistors to realize the adder function. Even though it has threshold loss problem, it is suited for low power design so far.

New adder design: Our new improved 14T adder cell requires only 14 transistors to realize the adder function shown in Fig. 6. It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate.

Newly proposed adders implement the Sum using XNOR-XNOR and Cout using PMOS-NMOS. We can also Build to produce Cout using NMOS-NMOS and PMOS-PMOS. But the delay and power dissipation of PMOS-NMOS is better than other two kinds of producing Cout. The proposed XNOR gate is designed by putting inverter at the output of the XOR gate in order to improve the threshold loss problem, which exists in the SERF adder. Out of the three methods, PMOS-NMOS based Cout gives the better result in power, speed and threshold loss problem.

RESULTS AND DISCUSSION

The present study have performed experiments on newly designed 1-bit full adders along with the SERF adder and the conventional CMOS adder at the schematic level. The transistors have a channel length of 2 u and a channel width of 1.9 u using 1.2 volt logic. Each circuit is simulated with the same testing conditions and the various results are shown in Fig. 7, 8 and Table 1, 2. The net lists of those adders are extracted and simulated using PSPICE on a Pentium IV machine.

Fig. 7 and Fig. 8 show the value of Sum and Cout for SERF and new improved 14 T Adder. The SERF does not provide logic 0 (approx 0.6 Volts) and logic 1 (approx 0.9 Volts) for sum and Cout for all possible input combinations. But the new improved 14 Tadder provides logic 0 (approx 0.3 Volts) and logic 1(1.2 volts) for sum and Cout for all possible input combinations. Thus the new improved 14T adder improves the threshold loss by 50% as compared to the SERF adder.

Table 1: Adder latency

Adder	Sum delay	Carry delay	Total delay
SERF	0.42	0.40	0.82
New	0.30	0.10	0.40

Table 2: Power dissipation (mW)

V_{dd}	SERF	New adder
1.2 V	303	0.010
1.1 V	183	0.008
1.0 V	91.6	0.006
0.9	30.5	0.005

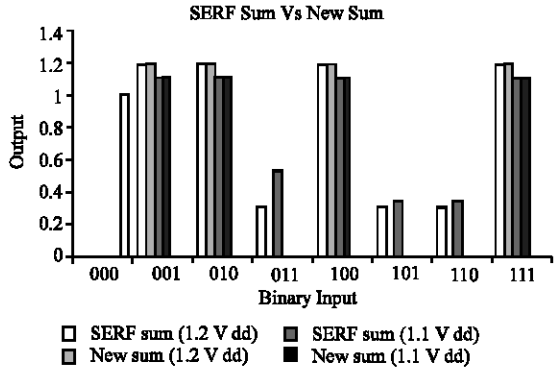

Fig. 7: Sum comparison

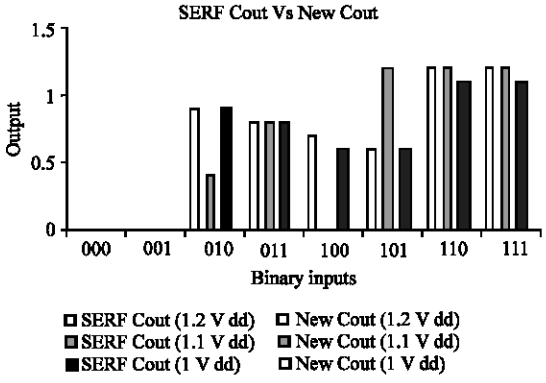

Fig. 8: Cout comparison

Propagation delay is the time between the fastest input signal and the output signal. We use the first rising edge of all signals at the beginning of the second pattern cycle. The results are shown in Table 1.

Table 1 shows that the new improved 14T adder has less latency than the SERF adder. Hence its speed is 48% more than the SERF adder at 1.2 V_{dd}.

Also the power dissipation of the SERF and new improved 14T adder at different Vdd are tabulated in Table 2.

From the Table 2 , we can conclude that the SERF recovers 303 mW at 1.2 V_{dd} and the new improved 14T adder dissipates only 10 μW. Hence we can build larger circuits with the help of our new adder cell which provides only small amount of power dissipation in the order of micro watts.

After the simulations, the new improved 14T full adders shown in Fig. 6 stand out as being the best. Along with the SERF adder and the other CMOS adders.

In power consumption at 1.2 V_{dd}, new improved 14T adder consistently has better power consumption as shown in Table 1. New improved 14T adder cell reduces the threshold loss problem by 50% as compared to the SERF adder. Also its speed is improved by 48% as compared to the SERF. Since our new adder cell dissipates small amount of power, we can call it as low power adder.

As mentioned earlier, the performance of many larger circuits are strongly dependent on the performance of the full adder circuits that have been used. The new improved 14-transistor adder circuits presented in this study are good candidates to build these large systems, such as high performance multipliers with low power consumption. The small increase in Transistor count of these adders can significantly reduce the latency of the systems built upon them.

CONCLUSIONS

The present study have presented a new improved 14T adder cell to construct full adders using only 14 transistors. Based on our extensive simulations, we conclude that our new adders consume considerably less power in the order of micro watts and have 48% higher speed and reduces 50% threshold loss problem compared to the previous different types of Transistor adders.

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